

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-37 are pending in this application. Claims 4-7, 10-13, 17-20, 23-26, and 31-34 were objected to as dependent upon a rejected base claim, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims. Applicants gratefully acknowledge that indication of the allowable subject matter.

Claims 2 and 29 are amended by the present response to delete the language noted as unclear, and thus the objections to claims 2 and 29 are believed to be overcome by the present response.

Claims 1-3, 8, 9, 14-16, 21, 22, 27-30, and 35-37 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 5,818,761 to Onakado et al. (herein "Onakado"). That rejection is traversed by the present response as discussed next.

Each of independent claims 1, 15, and 28 is amended by the present response to clarify language therein. Specifically, independent claims 1 and 28 now further recite "the second MOS transistor in a selected one of the memory cells being turned on when data is read from the first MOS transistor in the selected one of the memory cells". Independent claim 15 also recites that limitation and additionally recites "a second MOS transistor which has one end of its current path connected to one end of a current path of the first MOS transistor". Those claim features are believed to be fully supported by the original specification for example at page 21, line 11, to page 22, line 17.

According to the structure now clarified in each of independent claims 1, 15, and 28, a memory cell includes a first MOS transistor and a second MOS transistor. The second MOS transistor in the selected memory cell is turned on when data is read from the first MOS

transistor in the selected memory cell. That feature is believed to clearly distinguish over Onakado.

The outstanding rejection cites Onakado in Figure 10 to disclose first and second MOS transistors 24, the Office Action stating “the figure [10] actually shows 4 separate MOS transistors labeled as 24”.¹ Thereby, the Office Action appears to indicate the MOS transistors 24 in Figure 10 of Onakado correspond to both the first and second MOS transistors recited in the claims. Applicants respectfully submit the claims as written distinguish over such an interpretation in Onakado.

In Figure 10 in Onakado each MOS transistor 24 forms a memory cell. In Onakado when data is to be read from one of two MOS transistors 24, the other one of the two MOS transistors is *not turned on*. That is the case in Onakado because if the other one of the two MOS transistors was turned on, data from both of the two MOS transistors would be read out to one sub bit line, and that would result in a *failure* of a read operation.

In contrast to Onakado, in the claims as currently written the memory cells each include a first MOS transistor and a second MOS transistor, and when data is read from the first MOS transistor the second MOS transistor is turned on. Onakado does not disclose or suggest any such operation. Not only does Onakado not disclose or suggest such claimed features, but Onakado could not even have modified to meet such claimed features as Onakado teaches away from such claimed features, and would be *inoperative* for its intended operation if modified to meet such claimed features.

Thereby, the features recited in each of amended independent claims 1, 15, and 28, and the claims dependent therefrom, are believed to distinguish over Onakado. Thereby, those claims, and the claims dependent therefrom, are believed to be allowable over the applied art.

¹ Office Action of March 9, 2007, page 3, prenumbered paragraph 2, line 7.

In view of the present response applicants respectfully submit each of the claims as written distinguishes over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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